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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,725	01/07/2004	Rainer E. Gehres	FIS920030358US1	1724

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EXAMINER	
LINDSAY JR, WALTER LEE	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,725	GEHRES, RAINER E.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Election filed on 1/18/2005.

Currently claims 1-20 are pending. Claim 20 is withdrawn.

Election/Restrictions

1. Applicant's election without traverse of claims 1-19 in the reply filed on 1/18/2005 is acknowledged.

2. Claim 20 is withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected device, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 1/18/2005.

Drawings

3. Figure 1A should be designated by a legend such as --Prior Art—or –Background Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

5. Claims 2 and 16 are objected to because of the following informalities: the objective of the current invention seems to be limiting boron migration and would lead to the first FET of claim 1 to correspond to the PFET and the second FET would correspond to the NFET. Appropriate correction is required. The examiner will try to make a thorough examination of the claims.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1-3 and 6-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheek et al. (U.S. Patent No. 6,316,302 dated 11/13/2001) in view of Furukawa et al. (U.S. Publication No. 2002/0197806 dated 12/26/2002).

Cheek shows the method substantially as claimed in Figs. 1-4 and corresponding text as: forming gate stacks (22) of said integrated circuit over a substrate (10) (col. 2, line 55-col. 3, line 13); forming first spacers (24a, 24b) on sidewalls of said gate stacks (col. 2, line 55-col. 3, line 13); forming second spacers (24c) over said first spacers (col. 2, line 55-col. 3, line 13); forming source and drain regions (28) of said first FET in alignment with said second spacers of a first gate stack of said gate stacks (col. 2, line 55-col. 3, line 13); removing said second spacers (col. 3, lines 14-34); selectively etching said first spacers of a second gate stack of said gate stacks in a substantially vertical direction to remove horizontally extending portions of said first spacers (col. 3, lines 14-34); and forming source and drain regions (32) of said second FET in alignment with portions of said first spacers of said first gate stack which remain after etching (col. 3, lines 14-34) (claim 1). Cheek teaches that the first FET is an n-type FET (NFET) and said second FET is a p-type FET (PFET) (col. 2, line 55-col. 3, line 13) (claim 2). Cheek teaches that the gate stacks of the first and second FETs are aligned end-to-end in a horizontal direction over said substrate (fig. 1) (col. 2, line 55-col. 3, line 13) (claim 3). Cheek shows the method substantially as claimed in Figs. 1-4 and corresponding text as: forming a first gate stack (22) and a second gate stack (22) overlying a main surface of a substrate (col. 2, line 55-col. 3, line 13); forming a first spacer (24a,24b, 24c) on said first and second gate stacks, said first spacer having a vertically extending portion oriented in a direction generally perpendicular to said main surface, and a horizontally extending portion parallel to said main surface (col. 2, line 55-col. 3, line 13); forming source and drain regions (28) of said first FET aligned to said

first spacer of said first gate stack (col. 2, line 55-col. 3, line 13); removing said horizontally extending portion of said first spacer by a vertical etch process (col. 3, lines 14-34); and forming source and drain regions (32) of said second FET in said substrate aligned to said vertically extending portion of said first spacer of said second gate stack (col. 3, lines 14-34) (claim 15). Cheek teaches that the first FET is an n-type FET (NFET) and the second FET is a p-type FET (PFET) (col. 2, line 55-col. 3, line 13) (claim 16). Cheek teaches that the gate stacks of the first and second FETs are aligned end-to-end in a horizontal direction over said substrate (fig. 1) (col. 2, line 55-col. 3, line 13) (claim 17).

Cheek lacks anticipation only in not explicitly teaching that: 1) the first spacers by anisotropically etching of a second gate stack of said gate stacks in a substantially vertical direction to remove horizontally extending portions of said first spacers (claims 1 and 15); 2) forming a self-aligned silicide aligned to said source and drain regions of said NFET and said PFET (claims 6 and 18); 3) the etching is performed by a process including a reactive ion etch (claim 10); 4) the silicide is a silicide of cobalt (claim 13); and 5) forming a self-aligned silicide aligned to said gate stacks of said NFET and said PFET (claims 14 and 19).

Additionally, Cheek shows: forming source and drain extensions (40) of said NFET aligned to said gate stack of said NFET (col. 3, lines 35-47) (claim 7); forming a thin dielectric on said gate stack of at least said PFET and forming source and drain extensions (36) of said PFET aligned to said thin dielectric (col. 3, lines 14-34) (claim 8); the thin dielectric (24a) is formed by local thermal oxidation (col. 2, line 55-col. 3, line

13) (claim 9); the first spacers consist essentially of silicon nitride (24b) and said second spacers (24c) consist essentially of silicon dioxide (col. 2, line 55-col. 3, line 13) (claim 11); the first spacer consist essentially of silicon dioxide and said second spacers consist essentially of silicon nitride (col. 2, line 55-col. 3, line 13) (claim 12).

Furukawa shows a method using disposable and permanent films for diffusion and implantation doping. Sidewall spacers 135 are formed by conformally depositing a material, then anisotropically etching the material to remove materials on the horizontal surfaces but not on sidewalls or vertical surfaces. This is done with a Reactive Ion Etch (page 3, [0026]). Furukawa also shows that silicide (810) is formed on the gate and the source and drain regions, preferably cobalt silicide (page 4, [0040]). Methods employed by Furukawa are done to offset the detrimental effects associated with enhanced diffusion in extension regions and to aid in the reduction of series resistance in devices (page 1, [0005]).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method of Cheek by utilizing an anisotropic etch, such as reactive ion etch, and to grow cobalt silicide on the source/drain regions and gate, as taught by Furukawa, with the motivation that Furukawa teaches that by adding these features can offset detrimental effects associated with enhanced diffusion in extension regions and to aid in the reduction of series resistance in devices.

9. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheek et al. (U.S. Patent No. 6,316,302 dated 11/13/2001) in view of Madurawe (U.S. Patent No. 6,855,988 filed 4/14/2003).

Cheek shows the method substantially as claimed and as described in the preceding paragraph.

Cheek lacks anticipation only in not explicitly teaching that: 1) the substrate is a silicon-on-insulator substrate having an upper layer including a single-crystal semiconductor (claim 4); and 2) the single-crystal semiconductor consists essentially of silicon (claim 5).

Madurawe shows a method of forming a PFET and NFET devices on an SOI substrate. The first semiconductor geometry (850) forming the conducting paths for devices (810) and (820) can be a thinned down SOI single crystal Silicon film (col. 8, lines 49-60). The Thinned down SOI film allows for the device to have properties like a JFET device without a gate junction that would cause a reverse bias in the channel (col. 4, lines 50-64).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method of Cheek by utilizing a an SOI film with a single-crystal silicon layer, as taught by Madurawe, with the motivation that Madurawe teaches that the thinned down SOI film allows the device to behave like a JFET without a gate junction that would cause reverse bias in the channel.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
March 30, 2005